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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,911	10/01/2003	Gilles Amblard	H1553	8268
7590	03/01/2004		EXAMINER	
M. David Galin Renner, Otto, Boisselle & Sklar, LLP Nineteenth Floor 1621 Euclid Avenue Cleveland, OH 44115-2191			DANG, PHUC T	
			ART UNIT	PAPER NUMBER
			2818	
			DATE MAILED: 03/01/2004	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,911	AMBLARD, GILLES	
	Examiner	Art Unit	
	PHUC T DANG	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 24 October 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-4, 12, 13 and 15 is/are rejected.
- 7) Claim(s) 5-11 and 14 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 01 October 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 1003.
- 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

Art Unit: 2818

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on October 1, 2003 is acceptable.

Information Disclosure Statement

2. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on October 24, 2003.

Specification

3. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 12-13 and 15 are rejected under 35 U.S.C. 102 (e) as being anticipated by Young et al. (U.S. Patent No. 6,514,672 B2).

Young et al. discloses a method of forming an integrated circuit line on a wafer using a lithographic technique, comprising:

providing the wafer, the wafer including a substrate (10, Fig. 1) and, over the substrate, each of a photo resist layer (18, Fig. 2) and an underlying layer (16, Fig. 2) to be processed under the photo resist layer (18, Fig. 3);

exposing and developing the photoresist layer (18, Fig. 3) to form a photo resist line,

Art Unit: 2818

the photo resist line, the photo resist line having a line width smaller than a desired line width of the integrated circuit line;

coating the photo resist line (18, Fig. 6) with a reactive coating (20, Fig. 6); and
reacting the photo resist line with the coating (20, Fig. 6) to form a mask line having a line width corresponding to the desired line width of the integrated circuit line and with a smaller line edged roughness (LER) than of the photo resist line [col. 2, lines 46-col. 3, lines 61].

Regarding claim 2, Young et al. disclose a step of etching the underlying layer using the mask line to define formation of the integrated circuit line from the underlying layer [Fig. 6].

Regarding claim 12-13, Young et al. disclose the range of temperature of the wafer for reacting the photo resist line with the coating in the process [col. 2, lines 60-65].

Regarding claim 15, Young et al. disclose the integrated circuit line is a conductive line used to form at least one gate electrode or an addressable word line [Fig. 8].

5. Young et al. discloses the claimed invention except for the process parameters as claimed in claims 3-4. However, the selection of the claimed integrated circuit line parameters would have been obvious to one having ordinary skill in the art at the time the invention was made to improve a process for forming an integrated circuit line on a wafer, since it is well settle that when the general conditions of a claim are discloses in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Art Unit: 2818

Allowable Subject Matter

6. Claims 5-11 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tao et al. (U.S. Patent No. 6,174,818 B1) discloses Method of patterning narrow gate electrode.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is 571-272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-872-9306 for After Final communications.

10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang *PD*

Primary Examiner

Art Unit 2818

February 12, 2004